CAP LAYER ON GLASS PANELS FOR IMPROVING TIP UNIFORMITY IN COLD CATHODE FIELD EMISSION TECHNOLOGY

Government Rights

This invention was made with Government support under Contract No. DABT63-93-C-0025 awarded by the Advanced Research Projects Agency (ARPA). The Government has certain rights in this invention.

BACKGROUND OF THE INVENTION

The present invention pertains to a method for improving the uniformity of tip placement in cold cathode field emission technology and the improved product, particularly the cathode, resulting therefrom.

Field emission display (FED) technology utilizes a matrix addressable array of pointed, thin film, cold field emission cathodes in combination with a phosphor luminescent screen, as represented for example by U. S. Patent No. 5,210,472, the disclosure of which is incorporated herein by reference. An emissive flat panel display operates on the principles of cathodoluminescent phosphors excited by cold cathode field emission electrons. A faceplate having a cathodoluminescent phosphor coating receives patterned electron bombardment from an opposing cathode thereby providing a light image which can be seen by a viewer. The faceplate is separated from the cathode by a vacuum gap and, in some embodiments, the face plate and the cathode are

prevented from collapsing together by physical standoffs or spacers fixed between them. In some embodiments the cathode is integrally formed with a back plate, while in others the back plate is separate from the cathode, surrounds the cathode and is sealed to the face plate.

The cathode of a field emission display is comprised of arrays of emission sites (emitters) which are typically sharp cones that produce electron emission in the presence of an intense electric field. An extraction grid disposed relative to the sharp emitters provides the intense positive voltage for the electric field.

FEDs have heretofore required that high quality (and thus expensive) glass or single crystalline silicon be used for the cathode substrate. This requirement has been necessary to avoid shrinkage of the cathode substrate during subsequent processing and to prevent layers from delamination.

Current processes for making large area field emission flat panel displays are expensive due to several requirements, including having a cathode substrate with a flawless, smooth and flat surface with reasonable chemical durability. Another important parameter that must be considered is the above mentioned shrinkage problem. The shrinkage of the cathode substrate, after heat processing, is important when making a pattern on a large substrate as shrinkage causes misalignment between patterns on the substrate. Further still, the substrate from which the cathode tips (and circuitry therefor) is made, must traditionally contain no, or few,

impurities. Otherwise, during operations, the impurities will migrate into the tips or control circuitry, thus affecting performance. Therefore, expensive glass which is thermally matched to silicon, or single crystalline silicon, itself, has been traditionally used as the substrate on which a cathode is made. Therefore, there is a need for a less expensive substrate with reasonable quality for mass production of field emission displays.

An example of the prior art may be found in U. S. Patent No. 4,857,161, the disclosure of which is incorporated herein by reference.

SUMMARY OF THE INVENTION

The present invention concerns a method for improving the uniformity in tip location in cold cathode field emission devices, particularly those of large scale, by initially placing a cap layer on a cathode substrate, prior to processing and the resulting product. Thus the present invention has the ability to make more uniform silicon tips while substantially eliminating delamination of silicon layers.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be described by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic cross section through an FED in accordance with the prior art; and

Figure 2 is a schematic cross section through an FED in accordance with the present invention.

DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

Referring to Fig. 1, a field emission display 10 employing a cold cathode 12 and an opposing spaced anode 14 is shown. The cathode 12 has a substrate 16, which has been comprised of a glass matched to the characteristics of silicon, as explained above. The substrate 16 is coated with a conductive layer 18, such as amorphous silicon, microcrystalline silicon or polysilicon, and, at each emission site, conical micro-cathode emitters 20 are formed on the conductive layer 18. An insulator 22 separates a grid 24 from the conductive layer 18. The anode 14 is a transparent glass 26 coated with phosphors 28. This assembly is sealed in a package (not shown) and a high vacuum is drawn inside the package. The cathode 12, grid 24 and anode 14 are connected to electrical source 30. When a voltage differential, from source 30, is applied between cathode 12 and grid 24, a stream of electrons is emitted towards the phosphors 28 of the anode 14.

One example embodiment of the present invention improves the above-described display, shown in Fig. 1, by depositing a cap layer 32 directly on the surface of an inexpensive substrate 34, such as a soda-lime glass or plastics material substrate, followed by the conductive layer 36 from which tips 38 are formed. Examples of acceptable materials for the cap layer 32 include a silicon dioxide

(SiO_2), silicon nitride (Si_3N_4), silicon carbide or polycrystalline carbon. The cap layer need have a thickness of only 0.10 microns.

One acceptable method for making such a cap layer 32 is a plasma enhanced, chemical vapor deposition having the following process parameters:

SiH_4 = 100 standard cubic cm/min (sccm)

N_2O = 2000 sccm

N_2 = 900 sccm

Power = 900 watts

Pressure = 1 Torr

Temperature = 300°C

Next, Si film is deposited over the cap layer by the following process:

SiH_4 = 800 sccm

PH_3 = 8.0 sccm

Power = 300 Watts

Pressure = 1 Torr

Temperature = 300°C

or

SiH_4 = 800 sccm

B_2H_6 = 2.0 sccm

Power = 200 Watts

Pressure = 1 Torr

Temperature = 250°C

From this layer, cathode tips are fabricated according to many

alternative techniques (for example, as seen in U. S. Patent Nos. 5,229,331; 5,302,238; 5,372,973; and 5,391,259), all of which are incorporated herein by reference.

The advantage of the present invention is three fold:

1. The cap layer covers surface flaws in the glass substrate, which reduces concentration points of local stress and consequently results in more uniform tips.

2. The cap layer also serves as a diffusion barrier against certain contaminants that eventually could cause voids and valleys on the surface of the glass, and again result in tip non-uniformity.

3. The cap layer reduces glass shrinkage and thermal stress significantly. This is especially more evident when silicon tips are deposited on uncoated glass substrates where deposited films delaminate immediately after deposition due to very high thermal stress.

The forgoing illustrative embodiment has been discussed with reference to a glass substrate. It should be noted that the present invention is not restricted to glass but may be used with other inexpensive substrates, such as plastics or any other non conductive materials.

It should also be noted that it would be within the scope of the invention to include a leaching of sodium in the substrate to prevent sodium from moving into the cap layer.

It should be further noted that it is within the scope of the

present invention to include an anti-reflective coating or light blocking layer within the cap layer.

The present invention may be subject to many modifications and changes without departing from the spirit or essential, characteristics thereof. The present embodiment should therefor be considered in all respects as being illustrative and not restrictive of the scope of the invention as defined by the appended claims.